

ABSTRACT OF THE DISCLOSURE

A method of fabricating an X-ray detector array element. A gate and a gate insulation layer are formed on a substrate. A silicon island is formed on the insulation layer in a transistor area. A common line is formed on the insulation layer, simultaneously; source and drain are formed on the island to form a TFT. A bottom electrode is formed on the insulation layer in a capacitor area and covers the common line. A passivation layer is formed on the insulation layer, the bottom electrode and the TFT. A first via hole penetrates the passivation layer to expose the source. A planarization layer is formed on the passivation layer and fills the first via hole. Second and third via holes penetrate the planarization layer. The second via hole exposes the source. The third via hole exposes part of the passivation layer. A top electrode is formed on the planarization layer and connects the source.

I:\USER\YCSTE\DIV\APPL.SPEC.DOC